

EXHIBIT 6



Paper No. 25

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

IPR2022-00996

Patent 11,016,918 B2

**PETITIONER'S REPLY
TO PATENT OWNER'S RESPONSE**

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1001	U.S. Patent No. 11,016,918
1002	File History of U.S. Patent No. 11,016,918
1003	Declaration of Dr. Andrew Wolfe
1004	Curriculum Vitae of Dr. Andrew Wolfe
1005	File History of U.S. Provisional Application No. 60/941,586
1006	File History of U.S. Patent Application No. 12/131,873
1007	File History of U.S. Patent Application No. 12/240,916
1008	File History of U.S. Provisional Application No. 61/512,871
1009	File History of U.S. Patent Application No. 13/559,476
1010	File History of U.S. Patent Application No. 14/489,269
1011	File History of U.S. Patent Application No. 14/840,865
1012	File History of U.S. Patent Application No. 15/934,416
1013	[Intentionally Omitted]
1014	<i>SanDisk Corp. v. Netlist, Inc.</i> , IPR2014-00994, Paper No. 1 (PTAB June 20, 2014) (833 Patent IPR Petition)
1015	<i>SanDisk Corp. v. Netlist, Inc.</i> , IPR2014-00994, Paper No. 8 (PTAB Dec. 16, 2014) (833 Patent Institution Decision)
1016	<i>Smart Modular Techs. Inc. v. Netlist, Inc.</i> , IPR2014-01370, Paper No. 8 (PTAB Sept. 22, 2014) (833 Patent IPR Corrected Petition)
1017	<i>Smart Modular Techs. Inc. v. Netlist, Inc.</i> , IPR2014-01370, Paper No. 13 (PTAB Mar. 13, 2015) (833 Patent Institution Decision)

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1018	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00649, Paper No. 1 (PTAB Jan. 13, 2017) (833 Patent IPR Petition)
1019	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00649, Paper No. 7 (PTAB July 24, 2017) (833 Patent Institution Decision)
1020	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00692, Paper No. 1 (PTAB Jan. 17, 2017) (831 Patent IPR Petition)
1021	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00692, Paper No. 25 (PTAB July 5, 2018) (831 Patent Final Written Decision)
1022	<i>Micron Tech., Inc. et al. v. Netlist, Inc.</i> , IPR2022-00418, Paper No. 2 (PTAB Jan. 14, 2022) (833 Patent IPR Petition)
1023	U.S. Patent Application Publication No. 2006/0174140 to Harris <i>et al.</i>
1024	U.S. Patent No. 7,724,604 to Amidi <i>et al.</i>
1025	U.S. Patent Application Publication No. 2006/0080515 to Spiers <i>et al.</i>
1026	JEDEC Standard, DDR2 SDRAM Specification, JESD79-2B (January 2005) (“JESD79-2B”)
1027	JEDEC Standard, FBDIMM: Advanced Memory Buffer (AMB), JESD82-20 (March 2007) (“JESD82-20”)
1028	JEDEC Standard, FBDIMM Specification: DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification, JESD205 (March 2007) (“JESD205”)
1029	Declaration of Julie Carlson for JESD82-20 and JESD205
1030	U.S. Patent No. 7,719,866 to Boldo
1031	PCI Local Bus Specification Revision 2.2 (1998)

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1032	Mohan et al., Power Electronics: Converters, Applications, and Design (2d ed. 1995)
1033	U.S. Patent No. 7,721,130 to Prete <i>et al.</i>
1034	U.S. Patent No. 6,798,709 to Sim <i>et al.</i>
1035	[Intentionally Omitted]
1036	[Intentionally Omitted]
1037	U.S. Patent Application Publication No. 2008/0238536 to Hayashi <i>et al.</i>
1038	U.S. Patent No. 6,856,556 to Hajeck
1039	U.S. Patent Application Publication No. 2010/0257304 to Rajan <i>et al.</i>
1040	Texas Instruments, TPS51020 Datasheet (December 2003)
1041	Fairchild Semiconductor, FAN5026 Datasheet (October 2005)
1042	Murata Power Supply Reference Guide for Xilinx FPGAs (September 2006)
1043	Murata Power Supply Reference Guide for Altera FPGAs (February 2008)
1044	U.S. Patent Application Publication No. 2010/0205470 to Moshayedi <i>et al.</i>
1045	JEDEC Standard, Double Data Rate (DDR) SDRAM Specification, JESD79 (June 2000) (“JESD79”)
1046	JEDEC Standard, DDR3 SDRAM, JESD79-3A (September 2007) (“JESD79-3A”)
1047	U.S. Patent No. 7,023,187 to Shearon <i>et al.</i>

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1048	Murata, DC-DC Converter Specification (DRAFT), MPD4S014S Datasheet (Jan. 21, 2008)
1049	Micron, NAND Flash Memory Datasheet (January 2006)
1050	U.S. Patent No. 7,692,938 to Petter
1051	[Intentionally Omitted]
1052	[Intentionally Omitted]
1053	[Intentionally Omitted]
1054	[Intentionally Omitted]
1055	U.S. Patent Application Publication No. 2008/0101147 to Amidi
1056	U.S. Patent No. 5,563,839 to Herdt <i>et al.</i>
1057	U.S. Patent No. 6,693,840 to Shimada <i>et al.</i>
1058	Lenk, John D., <i>Simplified Design of Switching Power Supplies</i> (1995)
1059	U.S. Patent No. 7,061,214 to Mayega <i>et al.</i>
1060	U.S. Patent No. 5,630,096 to Zuravleff <i>et al.</i>
1061	Analog Devices, ADM1066 Datasheet (2006)
1062	Alan Moloney, <i>Power-Supply Management—Principles, Problems, and Parts</i> , Analog Dialogue (May 2006)
1063	National Semiconductor, LMC6953 PCI Local Bus Power Supervisor Datasheet (October 1996)
1064	U.S. Patent Application Publication No. 2007/0136523 to Bonella <i>et al.</i>
1065	U.S. Patent Application Publication No. 2009/0034354 to Resnick

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1066	U.S. Patent No. 10,672,458 to Shaeffer <i>et al.</i>
1067	LatticeXP Family Data Sheet (March 2006)
1068	Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, <i>Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.</i> , No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021)
1069	First Amended Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, <i>Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.</i> , No. 1:21-cv-01453 (D. Del. filed Jan. 18, 2022)
1070	Netlist's motion to dismiss the First Amended Complaint, <i>Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.</i> , No. 1:21-cv-01453 (D. Del. filed Feb. 16, 2022)
1071	Complaint in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021)
1072	Answer in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:21-cv-00463 (E.D. Tex. filed Apr. 12, 2022)
1073	Amended Complaint in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:21-cv-00463 (E.D. Tex. filed May 3, 2022)
1074	Email from counsel for Samsung to counsel for Patent Owner re: stipulation not to pursue certain invalidity defenses if an IPR proceeding is instituted
1075 [NEW]	Transcript of deposition of William Mangione-Smith, Ph.D. (June 12, 2023)
1076 [NEW]	Redline comparing Dr. Mangione-Smith's declaration in IPR2022-00996 (EX2031) to his declaration in IPR2022-00999 (EX2061)
1077 [NEW]	Netlist's Technology Tutorial

Exhibit #	Description
1078 [NEW]	Datasheet for ADP1821 Step-Down DC-to-DC Controller

CLAIM LISTING

Ref. #	Listing of Challenged Claims
1.a	1. A memory module comprising:
1.b	a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
1.c	a first buck converter configured to provide a first regulated voltage having a first voltage amplitude;
1.d	a second buck converter configured to provide a second regulated voltage having a second voltage amplitude;
1.e	a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;
1.f	a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and
1.g	a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising:
1.h	a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and
1.i	[1] at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, [2] the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices, [3] the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, [4] wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.
2	2. The memory module of claim 1, wherein the first and third buck converters are further configured to operate as a dual buck converter.

Ref. #	Listing of Challenged Claims
3	3. The memory module of claim 1, wherein the first voltage amplitude is 1.8 volts.
4	4. The memory module of claim 1, wherein the second, third, and fourth voltage amplitudes are 2.5 volts, 1.2 volts, and 3.3 volts, respectively.
5.a	5. The memory module of claim 1, further comprising:
5.b	a voltage monitor circuit configured to monitor a power input voltage received via a second portion of the plurality of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the power input voltage having a voltage amplitude that is greater than a first threshold voltage.
6	6. The memory module of claim 5, wherein the voltage monitor circuit is further configured to produce the trigger signal in response to the power input voltage having a voltage amplitude that is less than a second threshold voltage.
7	7. The memory module of claim 6, wherein the second threshold voltage corresponds to a voltage level that is ten percent less than a specified operating voltage.
8.a	8. The memory module of claim 1, the plurality of components further comprising:
8.b	[1] one or more registers coupled to one of the first, second, third and fourth regulated voltages, [2] the one or more registers configured to register, in response to a clock, the first plurality of address and control signals, [3] wherein the one of the first, second, third and fourth regulated voltages is selectively switched off to turn power off to the one or more registers while one or more components of the plurality of components are powered on.
9	9. The memory module of claim 5, wherein the first threshold voltage corresponds to a voltage level that is ten percent greater than a specified operating voltage.
10.a	The memory module of claim 5, the plurality of components further comprising:
10.b	a logic element including a non-volatile memory, the non-volatile memory is configured to store configuration information.

Ref. #	Listing of Challenged Claims
11	11. The memory module of claim 10, wherein, in response to the trigger signal, the logic element writes information into the non-volatile memory.
12.a	12. The memory module of claim 5, the plurality of components further comprising:
12.b	a non-volatile memory; and
12.c	a controller configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory.
13	13. The memory module of claim 5, wherein the power input voltage is coupled to the first, second, and third buck converters and the converter circuit.
14	14. The memory module of claim 8, wherein, in response to selectively switching on the one of the first, second, third and fourth regulated voltages to the one or more registers, the one or more registers is configured to output the registered first plurality of address and control signals to the plurality of SDRAM devices.
15.a	15. The memory module of claim 1, the plurality of components further comprising:
15.b	a logic element including one or more integrated circuits and discrete electrical elements, the one or more integrated circuit including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information.
16.a	A memory module comprising:
16.b	a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
16.c	first, second, and third buck converters configured to receive a pre-regulated input voltage and to produce first, second and third regulated voltages, respectively;

Ref. #	Listing of Challenged Claims
16.d	[1] a converter circuit configured to reduce the pre-regulated input voltage to provide a fourth regulated voltage, [2] wherein the first, second, third and fourth regulated voltages have first, second, third, and fourth voltage amplitudes, respectively;
16.e	a plurality of components coupled to the PCB, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages; and
16.f	a voltage monitor circuit configured to monitor an input voltage received via a first portion of the plurality of edge connections, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage.
17	17. The memory module of claim 16, wherein the second and third buck converters are configured to operate as a dual buck converter.
18.a	18. The memory module of claim 16, the plurality of components further including:
18.b	a controller coupled to the voltage monitor circuit and configured to receive the signal, wherein the controller executes a write operation in response to the signal.
19	19. The memory module of claim 18, wherein the write operation includes writing data information into non-volatile memory.
20	20. The memory module of claim 16, wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts.
21.a	21. The memory module of claim 16, the plurality of components further including:

Ref. #	Listing of Challenged Claims
21.b	<p>[1] at least one circuit coupled between the interface and the plurality of SDRAM devices,</p> <p>[2] the at least one circuit operable to receive a first plurality of address and control signals via a second portion of the plurality of edge connections and to output a second plurality of address and control signals to the plurality of SDRAM devices,</p> <p>[3] the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage,</p> <p>[4] wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.</p>
22.a	22. The memory module of claim 16, the plurality of components further including:
22.b	a logic element including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information, wherein the configuration information is used to program the logic element.
23.a	A memory module comprising:
23.b	a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
23.c	<p>[1] a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of first, second, third and fourth regulated voltages,</p> <p>[2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and one or more registers, the plurality of SDRAM devices coupled to the first regulated voltage, the one or more registers coupled to (i) the second regulated voltage, (ii) a portion of the plurality of edge connections, and (iii) the plurality of SDRAM devices,</p> <p>[3] wherein a plurality of address and control signals are coupled to the one or more registers via the portion of the plurality of edge connections;</p>
23.d	first, second, and third buck converters configured to provide the first, second and third regulated voltages, respectively; and

Ref. #	Listing of Challenged Claims
23.e	a converter circuit configured to provide the fourth regulated voltage,
23.f	wherein the second regulated voltage is configured to be selectively switched on or off to the one or more registers while at least the plurality of SDRAM devices are powered on,
23.g	wherein if the second regulated voltage is switched on while at least the plurality of SDRAM devices are powered on, the one or more registers are configured to couple the first plurality of address and control signals to the plurality of SDRAM devices, and
23.h	wherein if the second regulated voltage is switched off while the plurality of SDRAM devices are powered on, the one or more registers are configured to decouple the plurality of SDRAM devices from the first plurality of address and control signals.
24.a	24. The memory module of claim 23, further comprising:
24.b	a voltage monitor circuit configured to monitor an input voltage received from the host system via the interface, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage.
25.a	25. The memory module of claim 24, the plurality of components further including:
25.b	a controller coupled to the voltage monitor circuit and configured to receive the signal, wherein, in response to the signal, the controller executes a write operation.
26	26. The memory module of claim 25, wherein the write operation includes writing data information to non-volatile memory.
27	27. The memory module of claim 24, wherein the voltage monitor circuit is further configured to produce the signal in response to the input voltage having a voltage amplitude that is less than a second threshold voltage.
28	28. The memory module of claim 23, wherein the second and third buck converters are configured to operate as a dual buck converter.
29	29. The memory module of claim 23, wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts.

Ref. #	Listing of Challenged Claims
30	30. The memory module of claim 23, wherein the first, second, and third buck converters are configured to receive a pre-regulated input voltage and to provide the first, second and third regulated voltages, respectively, and wherein the converter circuit is configured to reduce the pre-regulated voltage input to provide the fourth regulated voltage.

I. INTRODUCTION

The Institution Decision (“ID”) correctly found all claims obvious. Netlist’s Patent Owner Response (“POR”) repeats many of the arguments that the ID already rejected.

II. ARGUMENT

A. There was no improper incorporation by reference (POR 1)

The Petition did not “improperly incorporat[e]” from the expert declaration, POR 1, but rather provided cross references *within the Petition* for later limitations that were nearly identical to earlier limitations and thus “obvious for at least the same reasons *above*,”¹ Pet. 50-51, 70-73, 123-26.

B. Construction of “memory module” (POR 1-3)

The Board properly found that Harris, the FBDIMM Standards, Amidi, and Spiers all disclose a “memory module,” ID 14-15, 17-18, 34-37, 45, as explained by the Petition, Pet. 19-20, 82-83; *see also infra* pp.23-26. After institution, the District Court held that “*memory module*” in the preamble is “[l]imiting,” EX2032, 35, consistent with the Board’s assumption, ID 18 n.2. Contrary to Netlist’s suggestion, neither the District Court nor Dr. Wolfe further limited “*memory module*” to only “*main* memory modules...designed to connect to the *primary* memory controller,” POR 2. *See* EX2032, 26-28, 35; EX2030, 125:12-127:13;

¹ Unless otherwise noted, emphases are added and internal quotes are omitted.

EX2056, 100:15-101:19.

C. Grounds 1-3 (POR 3-44)

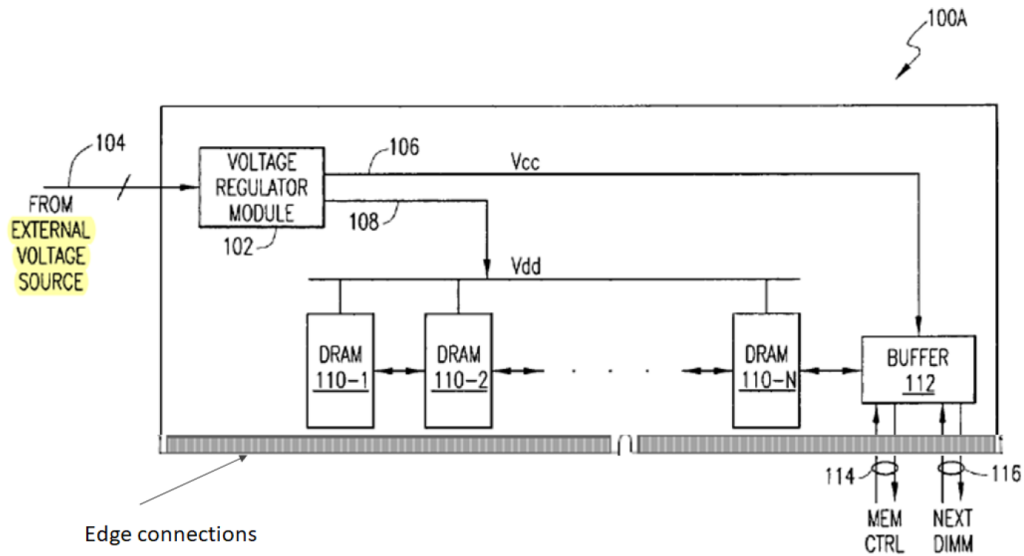
The Board properly rejected Netlist's arguments about Grounds 1-3. ID 13-41.

1. Ground 1 (Harris+FBDIMM Standards) discloses edge connections to receive power from the host system (POR 3-11)

The Board correctly found that Ground 1 (Harris+FBDIMM Standards) teaches "*edge connections configured to couple **power**...signals*," rejecting arguments similar to those repeated by Netlist here. ID 18-20; POR 3-11.

Netlist does not dispute that the FBDIMM Standards (part of Ground 1) teach supplying power via edge connections, Pet. 16-21, and Netlist's expert admits that such edge connections were "standard," EX1075, 97:16-98:18, 163:16-20; EX1077, 9.

Netlist argues that Harris's reference to "*externally* supplied voltage" (e.g., yellow below) requires power "external" to the *entire* "host system," POR 3-11, but Harris merely requires power "external" to the *DIMM memory module*, EX2030, 66:7-:19, 67:20-68:21, 91:22-92:7, 129:24-130:17; Pet. 21-22.



POR 5.

Netlist wrongly annotates Figure 1A (above) to suggest that Harris would *never* utilize edge connections at the bottom for power, POR 4-5, but Figure 3 of Harris, below, illustrates memory boards 306 coupled to the host system *only* through their edge connections (red), meaning power would also come from those edge connections:

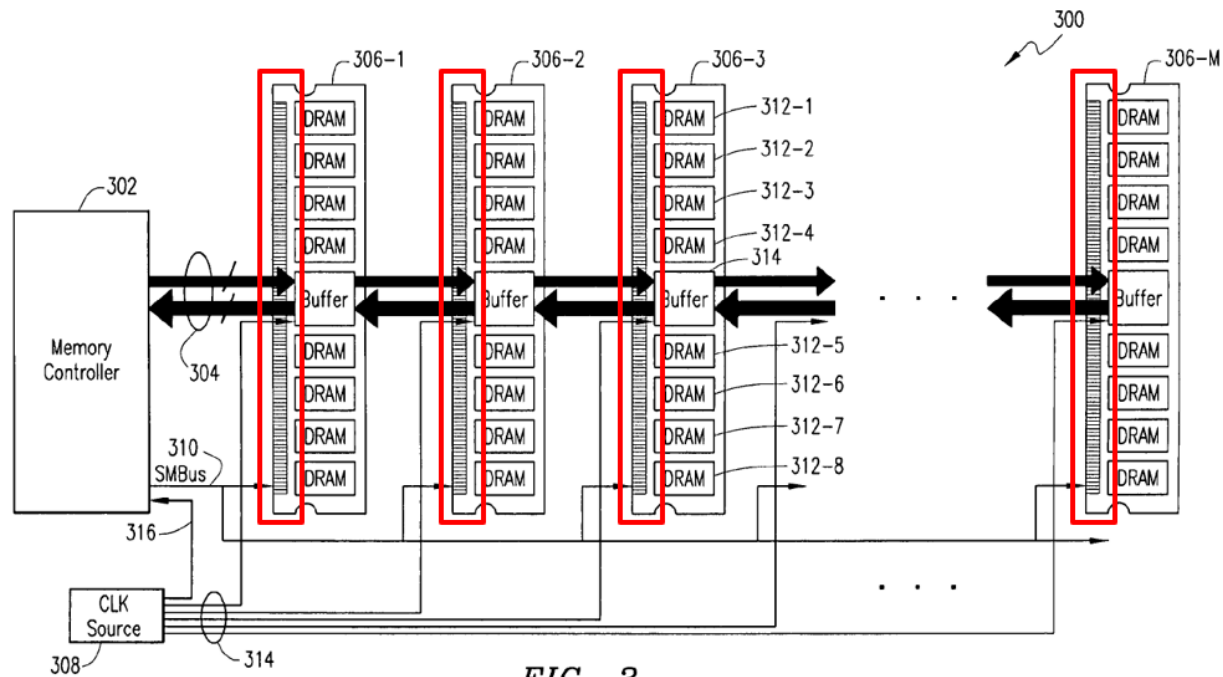


FIG. 3

EX1023, Fig.3. Indeed, Figure 3 of Harris above is nearly identical to a drawing by Intel where the memory modules admittedly receive power through the edge connections from the host system. EX1075, 171:4-:17; EX2101, 4. Harris also confirms that, “[a]lthough not explicitly shown in this FIGURE [3, above], each memory board also receives a supply voltage ...[which] may be sourced from the memory controller 302 [which is part of the host system, EX1075, 167:23-168:1] or from a separate voltage source.” EX1023, [0017]. As explained by Dr. Wolfe, it was common for the host to supply power through edge connectors “*alongside* the memory controller signals.” EX2030, 131:3-:5.

Netlist misinterprets paragraph [0019] of Harris to conclude that “system

board power supply...[is] eliminated” *entirely*. POR 4-5, 8, 10-11. To the contrary, Harris proposes avoiding the need for *different* system board voltages — such as “3.3V, 2.5V, 1.8V, 1.5V and beyond,” EX1023, [0002] — by simply supplying a *single* voltage (i.e., “12V”)² to the memory module, *id.* [0012-13], so that an “on-board voltage regulator module [e.g., 102 above] [can] generate appropriate local voltage levels” on the memory module, *id.* [0003]. As Dr. Wolfe explained, Harris’s “technology-independent voltage distribution scheme” eliminates the need for a “system-*board-specific* power supply,” *id.* [0019], not all power, EX2030, 116:10-117:6.

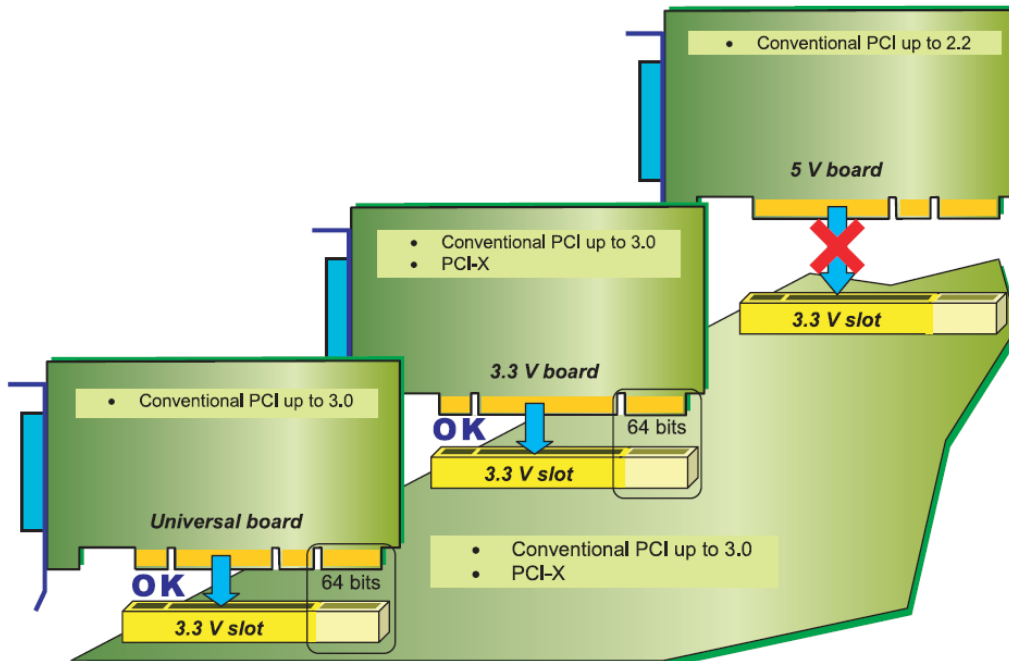
Using edge connectors like those illustrated in Figure 3 above to supply

² Netlist’s expert admitted that it was common at the time for the host system to provide a *regulated* “12V power supply.” EX2031, ¶65; EX1075, 180:14-183:3; EX2038, 8, 13. Netlist argues that Harris is limited to receiving an *unregulated* 12V supply, POR 6-7, when in fact Harris teaches that the input voltage can be “*regulated* or unregulated,” EX1023 [0014]. Indeed, both experts agree that Harris’s disclosure of a 12V supply with “wide tolerance (e.g., around +/-15%),” *id.* [0013], means that the voltage is *regulated* to stay within those limits. EX1003, ¶487; EX1075, 179:21-180:6, 183:7-184:11; EX2030, 65:23-66:6, 273:7-:12, 274:17-275:3.

power is also consistent with Harris's use of the known FB-DIMM ("FBD") design, except with "*few[er]*" power pins given the higher 12V input voltage. EX1023, [0012]; EX2030, 100:12-101:19, 102:17-:25, 103:11-104:23. To prevent "accidental damage" due to this change in the power pins of the edge connector, Harris teaches changing "the board's connector keyway" so that it is "not interchangeable with the standard DIMM." EX1023, [0013]; EX2030, 117:7-:21. This was a standard technique for memory modules receiving power *from the host* via the edge connections:

Signaling Voltage Interoperability

There is no way to mix 3.3 Volt and 5 Volt signaling voltage. The problem is solved thanks to the keying system of both the connector and the board.



EX2016, 6-7; *see also* EX2101, 21-22; EX1075, 171:21-175:20.

Netlist's argument that "[s]upplying power...from [the] *side*...was known,"

POR 5, misses the point: regardless of whether a side connection was *possible*, that would not negate the obviousness of using *edge* connections for power, as was highly common. *See Dome Pat. L.P. v. Lee*, 799 F.3d 1372, 1381 (Fed. Cir. 2015) (existence of a better alternative “does not mean that an inferior combination is inapt for obviousness purposes”). Indeed, Netlist’s expert admitted that using *both* was a known option, consistent with the combination for Grounds 2-3: the side connection could be used for battery backup (as taught by Amidi), and the edge connections could be used for power from the host system during normal operation (as taught by Harris):

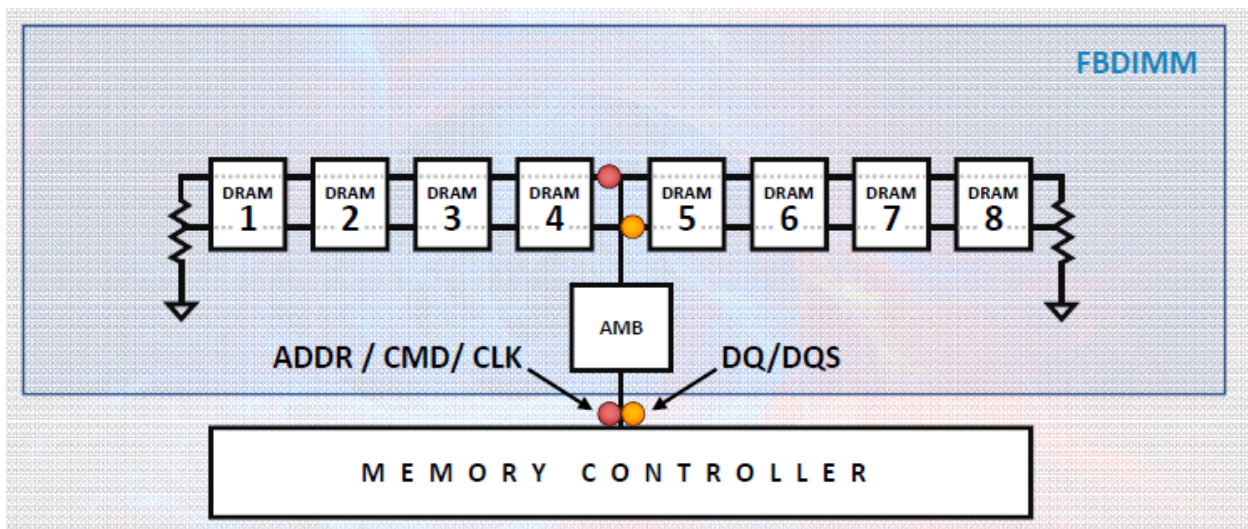
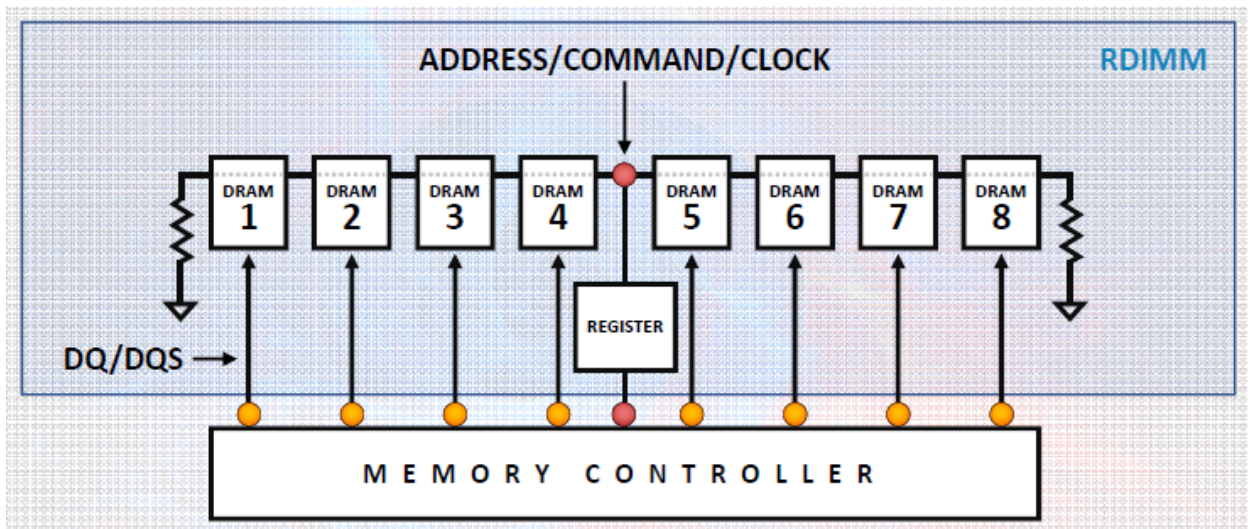


EX2035, 39; EX1075, 165:10-166:12.

2. Harris discloses receiving “data, address, and control signals” from the host (POR 11-15)

As shown below by Netlist’s technology tutorial, an FBDIMM (second below) receives *signals* for data (DQ), address (ADDR), and control (CMD),

similar to an RDIMM memory module (first below):



EX1077, 8-9; EX1075, 91:23-92:19, 95:14-96:13, 97:16-98:18.

Netlist incorrectly argues that Harris's FBDIMM (or FBD) does *not* receive data, address, and control "signals" from the host system because, under the FBDIMM standard, those signals are *encoded* first into a packetized signal that can be sent to the AMB (shown above) on fewer wires than if the signals were all sent separately. POR 11-12; EX2031, ¶31; EX1075, 155:22-157:1; EX2030, 8:3-11:6.

In essence, Netlist is trying to rewrite the claims (and its expert's testimony) to require "***dedicated*** pins" for address, command, and data, EX1075, 212:3-:8, 213:3-215:20, 219:13-220:9, 226:7-228:8, even though that is not what the claims say, and the specification specifically identifies FBDIMM as an embodiment of the invention. EX1001, 21:46-:55 ("fully-buffered (FBDIMM)"). Excluding a preferred embodiment from the claims is "rarely, if ever correct." *Kaufman v. Microsoft Corp.*, 34 F.4th 1360, 1372 (Fed. Cir. 2022).

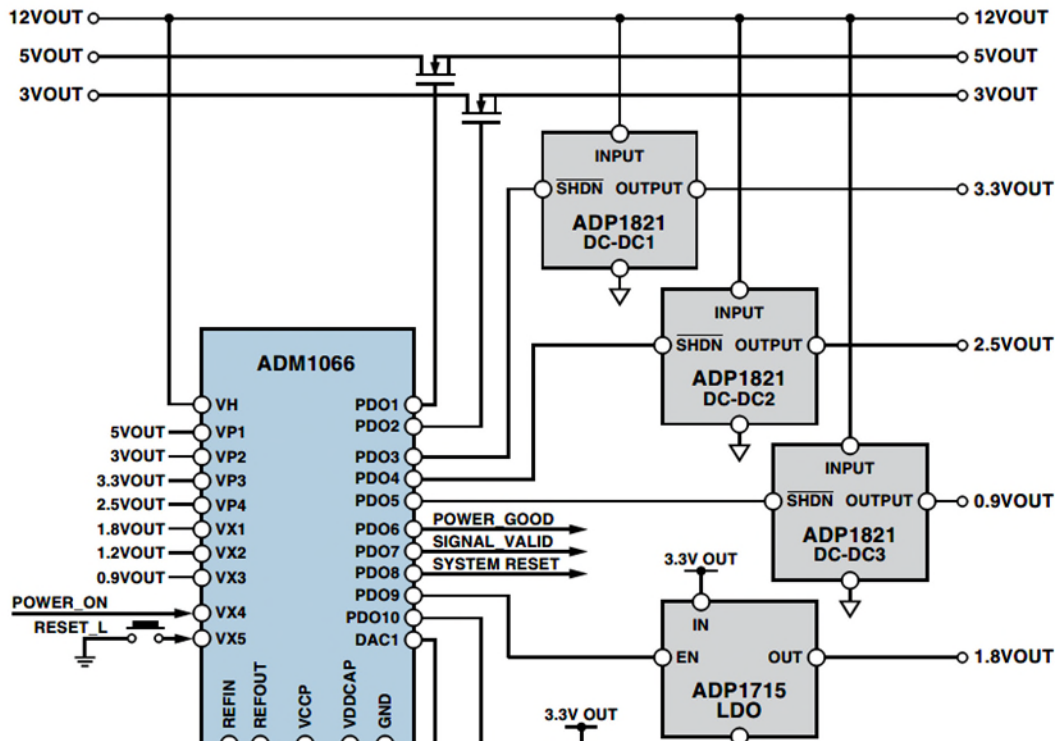
Indeed, Netlist concedes that the signals received by the AMB on the FBDIMM ***result*** in "data, address, and control ***signals*** needed by the DDR2 SDRAMs." EX2031, ¶31. And the FBDIMM standard confirms that "[a]ll memory control for the DRAM ***resides in the host***, including ***memory request initiation***," and the AMB "[a]cts as DRAM memory buffer for all ***read, write***, and configuration accesses addressed to the DIMM." EX1027, p.1. As a buffer for all such commands to the FBDIMM, the AMB must necessarily couple data, address, and control ***signals*** from the host system to the memory module.

3. Harris and the FBDIMM Standards render obvious using *four* converters (POR 15-31)

The Board correctly rejected Netlist's argument, repeated here, that it was not obvious to use ***four*** converters. ID 20-24.

a) Harris is not limited to one or two buck converters (POR 17-21)

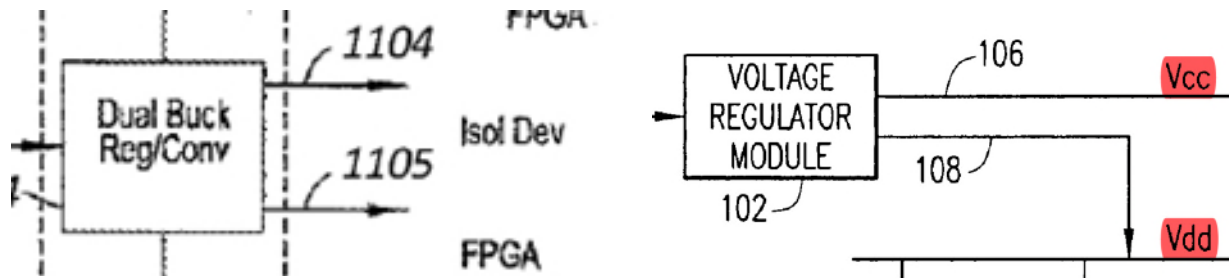
Netlist incorrectly argues that Harris only discloses “using a *single* converter.” POR 17. But buck converters were well-known switching devices commonly used to step down an input voltage to a lower output voltage. Pet. 28-30. Netlist’s expert agrees. EX1075, 103:21-107:14, 112:12-113:19. It therefore would have been obvious to a POSITA—and consistent with Harris—to use four converters (including three buck converters) to convert the 12V input to the required voltages on the memory board. Pet. 26-31; EX2030, 53:16-54:14. This was common, as shown below. EX1062, 15 (below, showing three buck converters labeled ADP1821 coupled to one 12V input to generate 3.3V, 2.5V, and 0.9V outputs); EX1075, 132:21-141:23; EX1078, 1 (ADP1821 datasheet).



Netlist’s argument that Harris only teaches a *single* buck converter is based on misreading the following sentence: “Preferably, a high-frequency switching voltage...may be implemented as the on-board VRM 102.” POR 17-18 (citing EX1023, Fig.1A, [0010]). But in a patent like Harris, “a” means “one or more,” see, e.g., *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342-43 (Fed. Cir. 2008), as confirmed by paragraph [0010] and claims 1 and 30 of Harris (“at least one” VRM).

Furthermore, Figure 1A of Harris (below right) is very similar to the “dual-buck converter” in Figure 16 of the 918 Patent (below left), which claims 2, 17, and 28 of the 918 Patent make clear count as *two* buck converters (given the two

different outputs, just like Harris), not one buck converter as Netlist now argues:

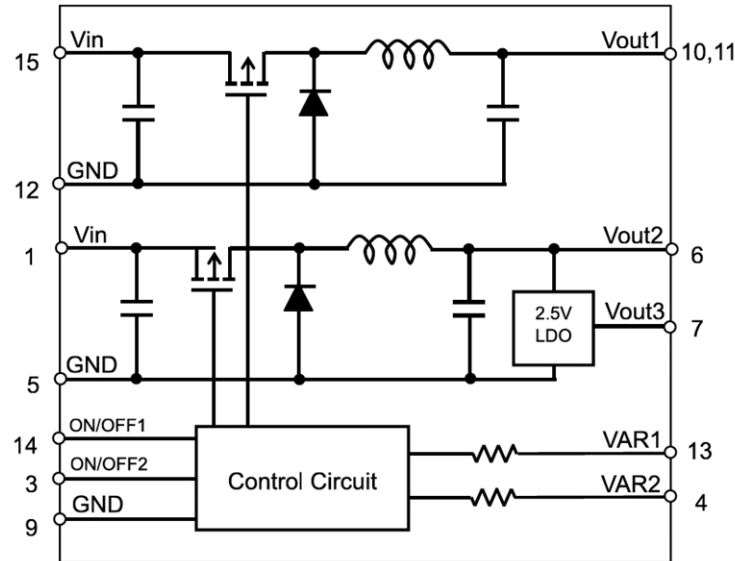


See also EX1075, 117:25-118:16. Indeed, the District Court, at Netlist’s urging, construed “dual buck converter” to merely require “two regulated voltage outputs.” EX2032, 18-21, 34; EX1075, 124:22-125:8, 126:9-:18; EX2030, 97:13-98:3. This further confirms that Figure 1A of Harris explicitly teaches at least *two* buck converters (for V_{CC} and V_{DD} , above right).

Netlist’s attempt to define the number of converters based on the number of “inductors” (POR 18-19) lacks any support. See generally EX1001 (not mentioning “inductor”); EX2032 (same). In any event, it was well known that a single chip can include multiple buck converters (and inductors). See, e.g., EX1048, 1-2 (“DC-DC converter”—singular—providing *two* regulated voltages, V_{out1} and V_{out2} , from *two* buck converters, shown below); EX1075, 106:24-109:8 (discussing use of inductor in a buck converter); EX2030, 98:8-:18 (same); EX1058, 5, 14-15 (similar).

DC-DC Converter Specification(DRAFT)

MPD4S014S



See also EX1075, 127:21-129:24, 228:25-232:19; EX1042, 16 (corresponding to EX1048, 2).

Finally, the alleged space required for multiple buck converters, POR 18-21, is not even mentioned in the 918 Patent or its claims, since solving any such problem was within the level of ordinary skill, EX2030, 53:16-54:14, 89:1-:21; *infra* pp.19-20.

b) It was obvious to use different converters for voltages that have different functions (POR 21-27)

The Board correctly found it obvious to use different buck converters for different voltages (e.g., V_{DD} vs. V_{DDL}). ID 22-24. JEDEC clearly teaches this as an option (e.g., red below) instead of using “a *single* power converter” for those

voltages (blue below):

2.3.1 Power-up and initialization sequence

The following sequence is required for POWER UP and Initialization.

- a) Apply power and attempt to maintain CKE below $0.2 \cdot VDDQ$ and ODT^{*1} at a low state (all other inputs may be undefined.) The power voltage ramp time must be no greater than 20mS; and during the ramp, $VDD > VDDL > VDDQ$ and $VDD - VDDQ < 0.3$ volts.

- VDD, VDDL and VDDQ are driven from a single power converter output, AND
- VTT is limited to 0.95 V max, AND
- Vref tracks $VDDQ/2$.

or

- Apply VDD without any slope reversal before or at the same time as VDDL.
- Apply VDDL without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.

at least one of these two sets of conditions must be met.

POR 25 (quoting EX1026, 9 (DDR2)); *see also* EX1046, 15 (same for DDR3).

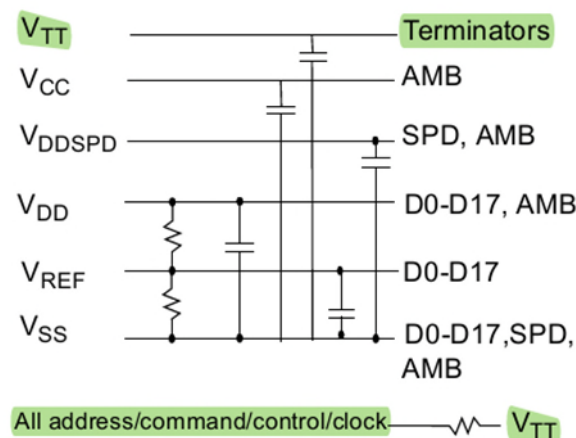
Netlist argues that using a *single* converter (as shown in blue above) was more common, POR 21-27, but the Petition explained the motivation for *multiple* converters (e.g., red above), including because the JEDEC standards treat those voltages separately, thus permitting power-on sequencing; providing independent control; improving efficiency; and saving power. Pet. 30-31; EX2030, 39:2-:10, 44:25-46:10; EX1075, 134:22-136:2, 194:23-195:7; EX1062, 13-15 (“sequence”/“sequencing”); EX2012, 73 (“sequencing”). The example Netlist provides with a “*single* power source” is *not* for an FBDIMM like Harris. POR 23 (citing EX2006, 4 (“SODIMM”)); EX1075, 102:17-103:9 (SODIMM is unbuffered as shown in EX2045 and EX2046, 4.20.11-23).

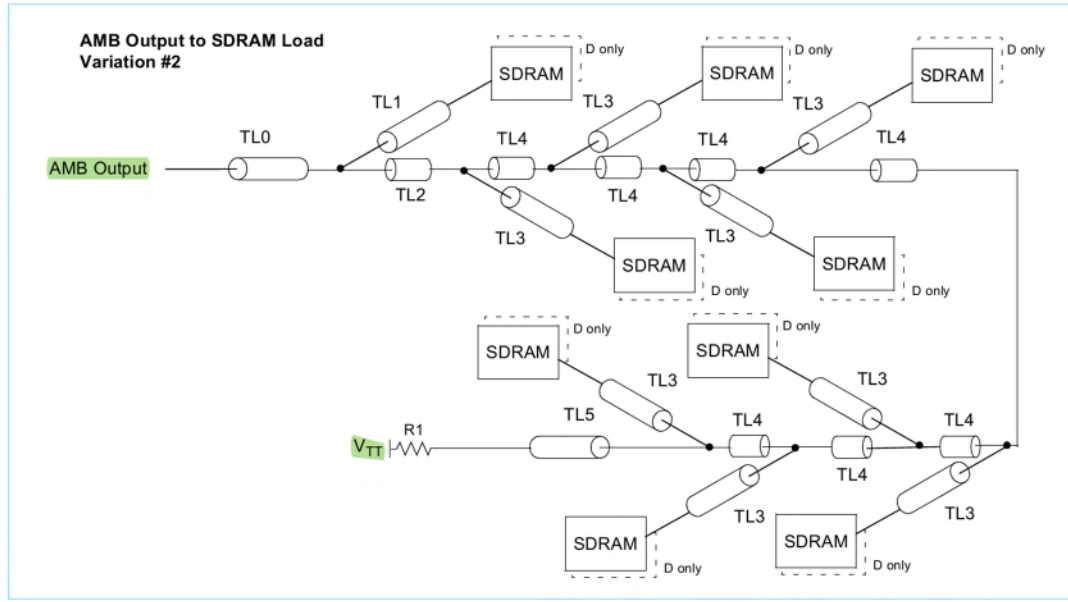
Netlist argues the JEDEC standard above is for the memory *device* (not module), POR 24-25, but Harris teaches a module that supplies all the voltages

needed on the module, which would include all those above needed by the memory devices. EX2030, 37:13-38:5. Similarly, Netlist argues that JEDEC’s express recommendation of *sequencing* the different voltages (red above) does not *require* separate converters, POR 24-27, but that was the obvious way, and came with several benefits as discussed above (including for V_{CC} vs. V_{CCFBD} , EX1003, ¶256).

c) It was obvious to use a third buck converter for V_{TT} (POR 27-30)

Netlist argues V_{TT} could be supplied from the motherboard, POR 27-30, but Harris teaches generating *all* the voltages on the module, including all of the voltages for an FBDIMM (“FBD”), which would include V_{TT} , as the Board found. ID 20-24; EX1023, [0012]; EX2030, 30:15-:20, 72:22-73:7, 103:11-104:23, 109:5-111:10, 239:8-:20. In particular, Harris’s module provides the voltages for the buffer 112 to send address and control signals to the DDR memory devices, which the FBDIMM Standards make clear require not just V_{DD} , but also V_{TT} to terminate those signals. Pet. 17-18; EX1028, 9, 15, 68 (below).





Furthermore, V_{TT} is required by JEDEC to “track” V_{DD} (which is clearly produced on Harris’s module, as shown in Figure 1A), which is why dual buck converters for generating V_{DD} and V_{TT} were readily available. EX1028, 9; EX2030, 72:22-73:7, 196:3-197:7 (citing EX1040-41, EX1048).



TPS51020

SLUS564B – JULY 2003 – REVISED DECEMBER 2003

DUAL, VOLTAGE MODE, DDR SELECTABLE, SYNCHRONOUS, STEP-DOWN CONTROLLER FOR NOTEBOOK SYSTEM POWER

APPLICATIONS


- Notebook Computers System Bus and I/O
- **DDR I or DDR II Termination**

EX1040, 1.

DUAL MODE AND DDR MODE

TPS51020 provides one-chip solution for system power supply, such as for 5 V, 3.3 V or 1.8 V, and a dual switcher DDR power supply. By simply selecting DDR signal and some external configuration change following the instructions below, TPS51020 gives a complete function set required for the DDR termination supply such as VDDQ/2 tracking V_{TT} source/sink capability and V_{TT} reference output.

Id. 11.



October 2005

FAN5026

Dual DDR/Dual-Output PWM Controller

- Complete DDR Memory power solution
 - VTT Tracks VDDQ/2
 - VDDQ/2 Buffered Reference Output
- Supports DDR-II and HSTL

Applications

- DDR V_{DDQ} and V_{TT} voltage generation
- Desktop computer
- Graphics cards

EX1041, 1.

Netlist also argues that an LDO linear regulator could generate V_{TT} instead of a buck converter, POR 29-30, but as shown above, buck converters were commercially available for V_{TT} and provided high efficiency compared to an LDO. EX1075, 112:12-114:8 (LDO may be only 10% efficient); EX2030, 57:17-:20, 58:18-59:10 (buck converters up to 98% efficient), 140:15-:24 (trend has been to use buck converters).

d) It was obvious to use a buck converter for V_{DDSPD} (POR 30-31)

Netlist argues that V_{DDSPD} (3.3V) could be supplied by the motherboard. POR 30-31. But Harris teaches generating *all* the voltages on the module, including all of the voltages for an FBDIMM (“FBD”), which would include V_{DDSPD} . EX1023, [0012]; Pet. 16-18. Netlist also ignores Ground 2, where the module switches to backup power and cannot rely on the motherboard for any power, including V_{DDSPD} . Pet. 52-56. In any event, “there are only two options” — from the motherboard, or from the module — rendering either obvious. ID 24.

Netlist also argues that an LDO would be used for V_{DDSPD} , instead of a buck converter. POR 31. But Netlist concedes the claimed “*converter circuit*” can be an LDO, POR 30 n.5, and in any event, using a buck converter (e.g., EX1048, 2) was an obvious, highly efficient, and clearly “suitable” option for converting 12V to 3.3V for V_{DDSPD} , EX1003, ¶¶146-49, 286; EX2030, 76:4-:19, 78:18-79:7, 79:24-80:11, 82:7-85:10, 88:4-:20, 89:1-:21, 138:14-:21, 140:15-:24, regardless of whether Netlist considers it “inferior” to an LDO, *Dome Pat.*, 799 F.3d at 1381.

4. It was obvious to combine Amidi’s battery backup with Harris (POR 31-38)

For Grounds 2-3, the Board correctly found a motivation to combine Amidi’s battery backup with Harris. ID 35-37; Pet. 52-56. Netlist argues Amidi was not needed because Harris already had a solution of redundant power supplies

to deal with power failures. POR 31-33. But Amidi provided a redundant power supply on the module itself — completely independent from the host — which differs from Harris’s redundant power sources that were provided by the host (and thus subject to the host losing power). Pet. 52-53; EX1003, ¶170; EX1024, 1:28-35, 2:6-26.

Netlist also argues that batteries had limitations and required space. POR 34-38. But such on-board battery backup systems were well-known at the time since their advantages “can be very helpful,” EX1024, 2:6-26, as evidenced by Amidi and Netlist’s own BBvault memory module from years earlier:

May 2005 1st BBvault shipped (battery-backed cache module). In production w/ 3rd generation.



BBvault

EX2035, 39; EX1075, 165:10-167:7. Furthermore, even if the battery backup takes one side of Harris’s FBDIMM, the other side can still include one rank, or even two ranks using *stacked* memory devices (which save space). EX1028, 36 (“Components shall be surface mounted on *one* or both sides of the PCB.”);

EX1075, 74:22-75:25 (“you’ve now doubled the amount of memory stored in the same amount of physical space”), 77:10-:17.

5. Grounds 1-3 disclose “*pre-regulated input voltage*” (POR 38)

For claims 16-22 and 30, the Petition correctly identifies a “*pre-regulated input voltage*” to each converter, *see* Pet. 73-75, such as Harris’s “regulated” 12V input under the Board’s interpretation of the claim, EX1023, [0013-14]; ID 37-38.³

6. Overvoltage protection in claims 5, 16, 24 and dependents (POR 38-42)

The Board correctly found *over*voltage protection in claims 5-7, 9-13, 16-22, and 24-27 obvious in light of Grounds 2-3. ID 38, 40-41. Netlist incorrectly argues that the Petition failed to show “that a POSITA would have been motivated to detect input over-voltage” and switch to backup power in response, POR 40-42, ignoring the Petition’s extensive explanation and evidence about a POSITA’s

³ The District Court construed “pre-regulated input voltage” to have its plain and ordinary meaning, EX2032, 21-22, 34, similar to the Board, ID 37-38, and rejected Samsung’s argument that the voltage must be pre-regulated *on* the memory module, EX2030, 268:18-270:5. Netlist’s expert does not dispute the District Court’s construction. EX1075, 142:10-144:18. Both experts agree that the 12V input to Harris can be pre-regulated under that construction. *See supra* p.5, note 2.

understanding of how to handle power anomalies, including both under- and over-voltage conditions, with a reasonable expectation of success. *See, e.g.*, Pet. 12-13, 60-66, 75-77; EX1003, ¶¶137, 180-87, 363-84. The Petition also explained how Amidi, in combination with Harris (Ground 2) and Hajeck (Ground 3), teaches a trigger signal to switch to back-up power and avoid data loss in case of a “power fault,” including under- and over-voltage conditions. *Id.*; *see also* Pet. 60-63; EX1003, ¶¶368-75; EX2030, 226:16-:22, 230:17-232:6, 251:10-254:2 (explaining Hajeck). Netlist’s arguments to the contrary attack the references individually (e.g., for lacking a trigger signal), while ignoring the proposed combinations. POR 39-42.

Netlist argues the prior art only solved ***undervoltage*** problems. POR 38-42. To the contrary, Harris expressly teaches that its memory module can “***accommodate***” up to a 15% variation above and below the nominal 12V supply voltage, EX1023, [0013], which would have motivated a POSITA to detect when the voltage is outside of the +/-15% tolerance not accommodated by Harris’s module, EX1003, ¶¶366-75. And Amidi teaches “power fault detection” for memory modules in general, with undervoltage detection being only an example. EX1024, Title, Abstract, 2:6-:19 (“power fault detection for a memory module may be provided in a variety of ways”). Dr. Wolfe explained that a POSITA understood the dangers of both under- and overvoltage. EX1003, ¶¶371-73;

EX2030, 254:24-256:11, 258:12-:20; EX1065, [0018-19] (alarm signal when voltage is outside of a range, including upper and lower thresholds); EX1063, 1-2 (PCI Power Supervisor detecting Over-, Under-, and out-of-window voltage faults); EX1061, 15 (similar); EX1062, 15 (similar). Netlist’s expert agreed that power spikes were known power anomalies at the time. EX1075, 196:10-197:13.

Netlist argues that overvoltage poses no danger. POR 40-42. But the Petition explained, e.g., with reference to Hajeck, the problems caused by over-voltage anomalies, such as power surges, that can cause data loss, data corruption or circuitry damage in memory boards — as anyone with a surge protector at home knows. Pet. 75-76; EX1003, ¶¶137, 184. As discussed above, Harris also discloses that its module can accommodate only +/-15%, which is consistent with some commercial converters requiring a V_{CC} input voltage with a 5% tolerance for proper operation and an absolute maximum of 30% overvoltage “beyond which the device may be damaged.” EX1041, 4 (below in part).

Absolute Maximum Ratings

Absolute maximum ratings are the values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Parameter	Min.	Typ.	Max.	Units
VCC Supply Voltage			6.5	V
VIN			18	V

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage VCC		4.75	5	5.25	V
Supply Voltage VIN				16	V

7. Non-volatile memory for claims 10-11, 15, 22 (POR 43)

The Petition explained that the “non-volatile memory” for the “logic” can either be in Harris’s Buffer (e.g., an AMB) or in an SPD connected to that Buffer. Pet. 47-50, 67-68, 72; EX2030, 285:3-286:17. Netlist argues it cannot be in an SPD—contrary to the Board’s finding, ID 31-33—because the SPD is a “different component[]” from the AMB, POR 43. But Netlist’s argument is contrary to the specification, which provides that the “logic” can be “*one or more* integrated circuits,” EX1001, 23:1-18, meaning the “logic” could comprise an SPD (with non-volatile memory) connected to an AMB, Pet. 47-49. Netlist also argues that standard AMBs did not include non-volatile memory, ignoring the obviousness of such a design, particularly in combination with Amidi. EX1003, ¶¶434-36.

8. Write operation for claims 11-12, 18-19, 25-26 (POR 43-44)

Netlist argues S3 mode would not be used when there is an *over*voltage condition. POR 43-44. But as explained above (pp.20-22), *over*voltage conditions can also cause data loss, thus motivating a POSITA to switch to backup power, where S3 mode would be used. Pet. 68-69.

D. Grounds 4-5 (POR 44-76)

1. Spiers’s PCI card is a “*memory module*” (POR 44-48)

The backup device 144 in Spiers, which is implemented in the PCI card shown in Figure 5, satisfies the District Court’s construction for “*memory module*” discussed above (pp.1-2) because it connects over a “bus” to a “memory

controller” in the “storage controller” 132, which sends memory commands to the backup device 144, as shown below. EX2030, 213:1-:8, 213:14-:22, 206:6-207:13.

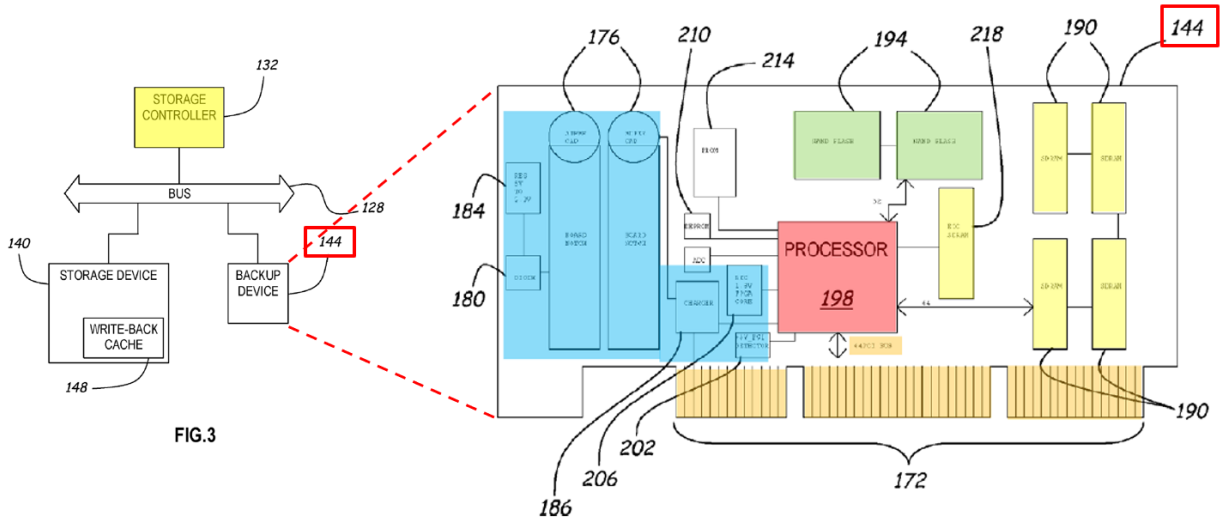
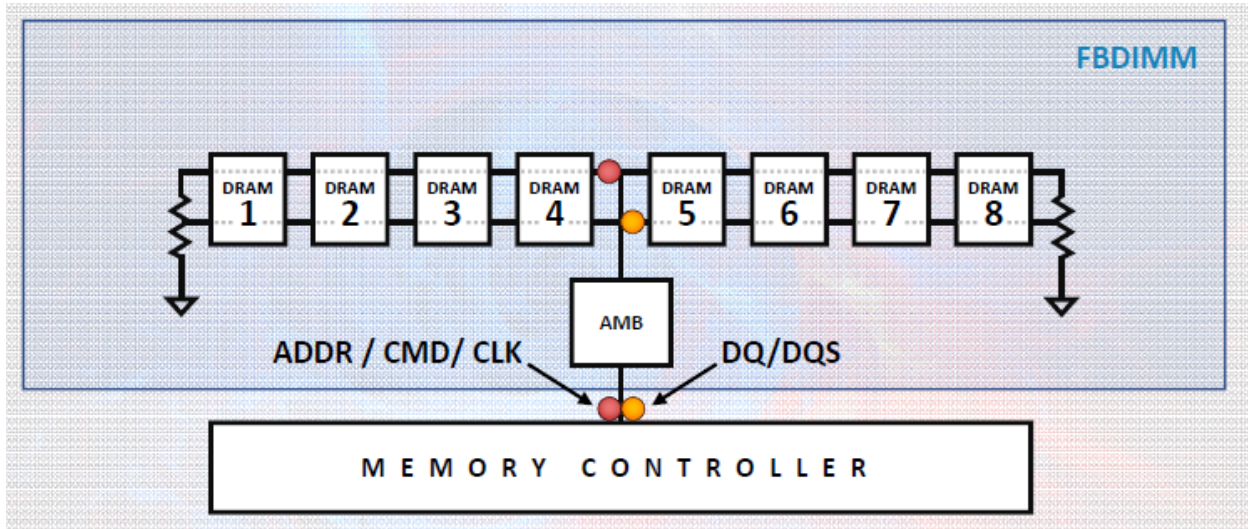


FIG.5

EX1025, Figs.3, 5, [0034] (“[T]he storage controller 132 [in Fig.3 above left] stores a copy of the data in the backup device 144....[and] periodically flushes the data stored in the backup device 144....”); EX1003, ¶¶644-45; Pet. 82-83.

Indeed, it was well known that PCI cards could be “memory modules,” as recognized by the PCI standard itself. EX1031, 1 (“The [PCI] bus is intended for...processor/*memory* systems.”), 22-25 (describing Memory Read and Write commands); EX2030, 177:25-179:9. Netlist concedes that parts of Spiers’s PCI backup device 144 (e.g., SDRAM 190 or flash modules 194) “include the necessary structure to connect to a memory controller.” POR 45. Netlist’s position appears to be that the intervening processor 198 on Spiers’s PCI card prevents the PCI card from functioning as a “memory module,” but the use of an

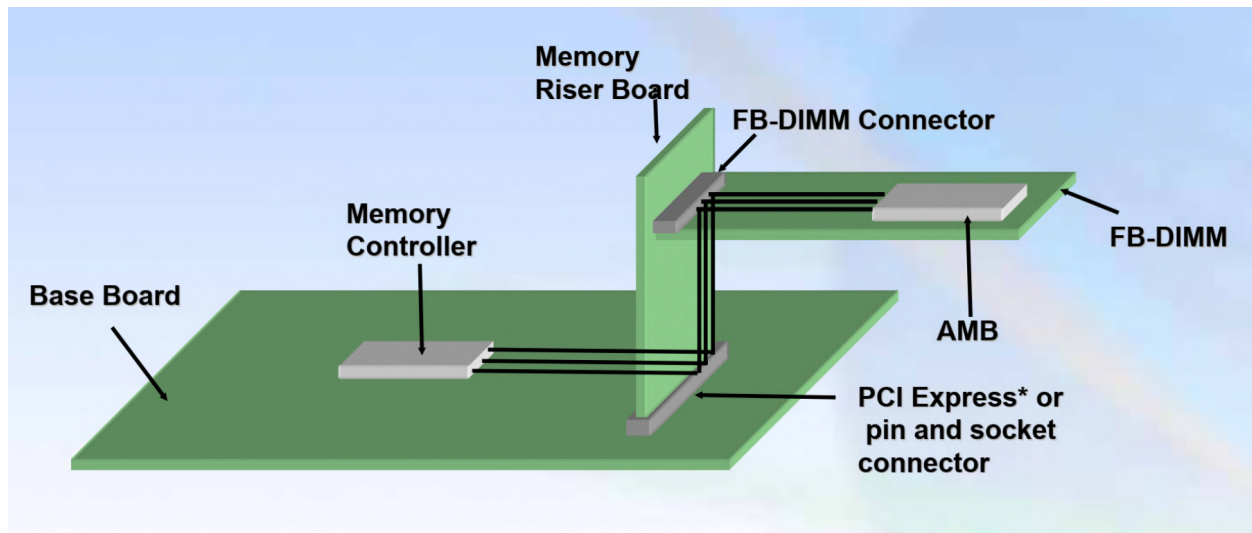
intervening processing unit on the “memory module” that is configured to interact with the “memory controller” of the host system is a common feature of well-known “memory modules,” such as an FBDIMM (below), where the “AMB” has an interfacing function similar to processor 198 in Spiers’s PCI card:



See EX1077, 9; EX1075, 97:16- 98:18; see also *id.* 91:23-92:19, 95:14-96:13 (similar for RDIMM). As discussed above (pp.8-9), FBDIMM is a disclosed embodiment of the 918 Patent, so excluding it from the scope of the claims would “rarely, if ever [be] correct.” For similar reasons, it would be incorrect to exclude Spiers’s PCI card from the scope of the claims simply because it has a “processor” on the module (similar to the AMB on an FBDIMM) that interacts with the “memory controller” in “storage controller” 132.

Lastly, Netlist is wrong to suggest that the *slot* used for a PCI card precludes the PCI card from being a “memory module.” POR 46-47. Neither the District

Court's construction for "*memory module*" (pp.1-2) nor the 918 Patent puts any limitations on the form factor or connector used by the memory module. *See, e.g.*, EX1001, 21:51-:55. Netlist's own exhibit includes an example configuration where a memory controller communicates with an FBDIMM through a PCI bus using a PCI connector:



EX2101, 14; EX1075, 198:11-200:7. This further confirms that a PCI card (such as Figure 5 of Spiers) can be used in conjunction with a memory controller in the host system.

2. Spiers+Amidi renders obvious four regulated voltages (POR 48-59)

The Board correctly found that Grounds 4-5 (with Spiers+Amidi) render obvious *four* regulated voltages. ID 46-50; Pet. 86-93.

a) Spiers is not limited to older SDR SDRAM memory (POR 48-52)

Netlist does not dispute that DDR2 and DDR3 were well-known types of

SDRAM, and that Amidi teaches the use of DDR2 SDRAM memory devices. Pet. 32, 78-79, 94. But Netlist nonetheless asserts that a POSITA would not consider DDR2 and DDR3 to be suitable for use with Spiers. POR 48-52. The Board correctly rejected this argument. ID 49-50.

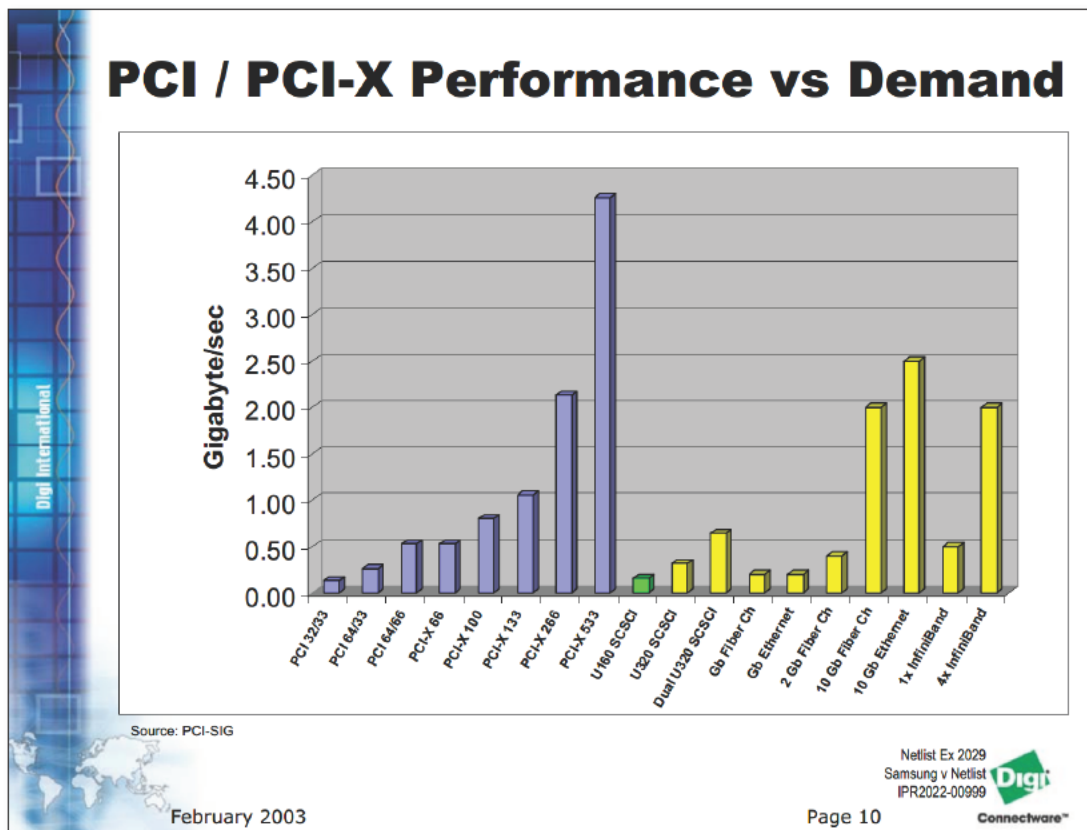
The only basis for Netlist’s argument appears to be the specific voltages disclosed in Spiers. POR 48-52. Netlist repeatedly emphasizes that Spiers suggests using a 3.3V regulator, while DDR2 and DDR3 use lower voltages. *Id.* 49 (citing EX1025, Fig.5, [0037]). But lower voltages are a “*motivation*” for using DDR2 or DDR3—not a problem—because that would “lower[] the power consumption.” EX1075, 79:9-80:2.

b) It would be obvious to use newer, more efficient DDR2/DDR3 memory (POR 53-69)

Netlist’s assertion that a POSITA would not be motivated (e.g., by Amidi) to use the faster and more advanced DDR2 or DDR3 devices in Spiers defies logic. It is well established that DDR2 and DDR3 provide substantial upgrades in speed and performance compared to older approaches like SDR. *See* EX2012, 70 (“less heat...more efficiency”), 73 (“usage is expected to increase to 80 percent [of all electronic systems]”); EX2030, 150:14-151:16, 180:8-182:11, 183:24-184:9, 245:4-246:8 (listing benefits for using newer DDR2 or DDR3 SDRAMs on Spiers’s PCI card); *see also* EX1075, 86:12-89:11 (faster “clock speed”). And the Federal Circuit has recognized that there is “an implicit motivation to combine to

make a device more desirable, for example because it is...faster...or more efficient.” *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 797 (Fed. Cir. 2021) (rejecting Board’s contrary finding).

Netlist’s argument that the PCI connections in Spiers eliminate any need for the faster speeds provided by DDR2 or DDR3 is also incorrect. POR 55-56. Netlist’s expert admitted that there were known, faster versions of PCI, shown below in purple, that “could be used in systems that use any of those technologies [including Ethernet] without necessarily being a bottleneck[.]” EX1075, 59:13-:23.



EX2029, 10. Given that the newer iterations of PCI could take advantage of the

faster speeds provided by DDR2 and DDR3, and were intended to be backwards compatible, EX1075, 52:8-:25, 53:25-54:23, a POSITA would have been motivated to implement those approaches in Spiers.

In addition to ignoring the level of skill at the time, Netlist's arguments are also incorrect legally because it is not necessary to show that using DDR2 or DDR3 would be the "*best*" implementation of Spiers, just that they were a "*suitable* option." *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380-81 (Fed. Cir. 2023) (reversing Board); ID 44.

3. It would be obvious to use four buck converters with Spiers+Amidi (POR 60-69)

The Board correctly found that Grounds 4-5 (with Spiers+Amidi) render obvious using *four* buck converters. ID 46-50; Pet. 86-93.

a) Buck converter for V_{TT} (POR 60-63)

Netlist argues Spiers would not include V_{TT} because that voltage is (according to Netlist) only used for DDR3 devices in AC measurements and tests. POR 60-61. To the contrary, as discussed above (pp.15-17), a memory module (like Spiers's) with on-board power generation needs to use V_{TT} to terminate the address and control signals sent from the module's local controller to the DDR2/DDR3 SDRAM devices. *See also* EX1003, ¶¶680-81, 683; EX1046, 15 (DDR3: "Apply VDDQ...before or at the same time as VTT & Vref"); EX1026, 9 (same for DDR2); EX1047, 2:7-15 ("In...a dual-data-rate (DDR) memory

system...a second supply voltage will be...one-half[] of a first supply voltage.”), 5:56-59 (“Vout2 may provide a VTT supply voltage”).

Netlist’s argument that Spiers is not an FBDIMM misses the point in the Petition. POR 62. The Petition referenced FBDIMM to explain that Spiers’s processor 198 is interfacing with the SDRAM memories on the module “just like in an FBDIMM,” creating the need for V_{TT} . Pet. 87-88; EX1003, ¶¶682-84. Finally, Netlist argues that an LDO could be used instead of a buck converter, POR 62-63, but as discussed above (pp.16-17), efficient dual buck converters were commercially available for V_{DD} and V_{TT} .

b) Multiple 1.8V buck converters (POR 63-64)

Netlist argues that a 1.8V voltage for V_{CCFPGA} and V_{DD}/V_{DDQ} could be provided from the same converter. POR 63-64. But as discussed above (pp.10-11, 13-15), a POSITA understood that using separate buck converters was a readily available and obvious design choice that provided a number of advantages, including efficiency, flexible sequencing, power control, and power savings. Even if an alternative implementation could be configured with a single converter, this does not make the use of separate converters non-obvious. *See, e.g., PACT XPP*, 61 F.4th at 1380-81 (“suitable option”); *Dome Pat.*, 799 F.3d at 1381.

c) Two buck converters for 1.5V and 1.8V (POR 64-65)

Netlist’s arguments regarding the use of two converters for 1.5V and 1.8V

are wrong for at least the same reasons stated in the section directly above regarding the use of multiple buck converters outputting 1.8V.

d) Buck converter for 5V-to-3.3V (POR 65-69)

Netlist argues it was not obvious to implement Spiers's 5V-to-3.3V regulator as a buck converter because an LDO would be sufficient based on its expert's calculation. POR 65-69 (citing EX2031, ¶¶163-71).⁴ That calculation, however, ignores the advantages of a buck converter, including efficiency and the capability to provide high currents, and is based on incorrect assumptions, such as basing the calculation on a write-back cache (like 148, orange below), *see* EX2031, ¶166, instead of Spiers's backup device 144 (green below).

⁴ Netlist also incorrectly asserts that the 5.5V-to-3.3V regulator 184 in Spiers is only "for use '*in the event of a power failure.*'" POR 65. But as Dr. Wolfe explained, regulator 184 is also used in normal mode. EX2030, 149:11-150:1 ("you're always using 184 because what's being monitored is the 5 volt supply, not the 3.3 volt supply, and the 5 volt supply feeds into 184"); *see also id.* 154:22-156:15, 156:23-157:8, 278:5-:15 ("it would...be obvious to have the regulator operate all the time"), 278:17-281:17 ("all the indications in Spiers [including diode 180] are that that 3.3 volts comes from the 5 volt to 3.3 regulator [184]"), 282:7-:14.

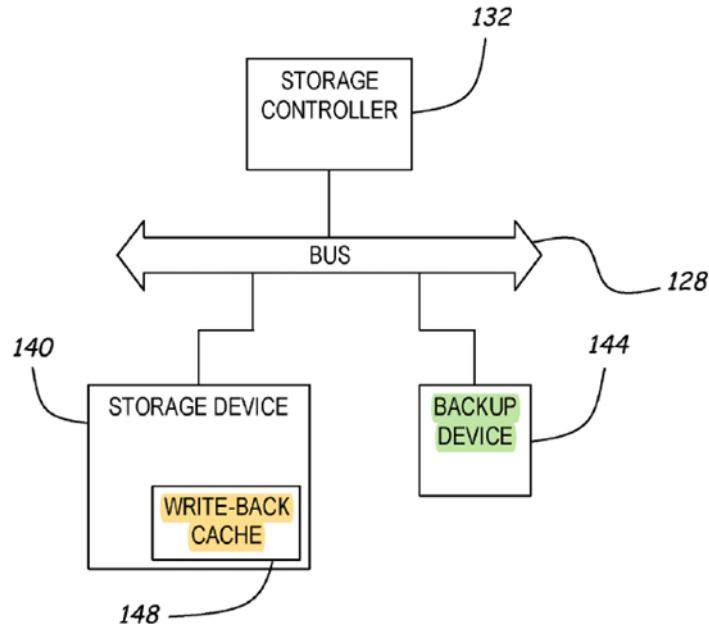
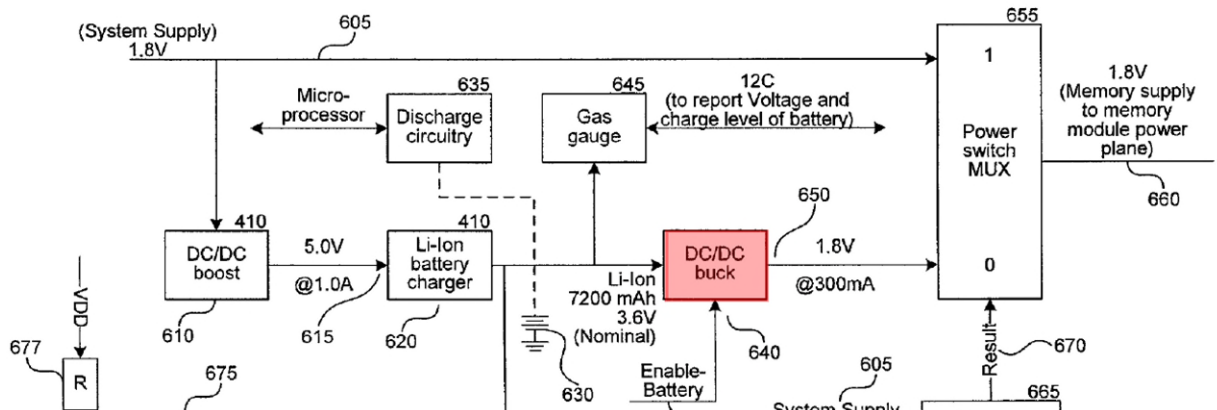


FIG.3

EX1025, Fig.3; EX1075, 208:20-209:1. Furthermore, using a buck converter for battery backup power is expressly taught by Amidi:



EX1024, Fig.6; Pet. 91. Netlist also argues that low-dropout buck converters had “drawbacks,” POR 67-69, but reliable buck converters for 5V-to-3.3V were commercially available at the time, *e.g.*, EX1048, 3 (requiring minimum input of

4.5V, minimum voltage drop of 1V, and minimum load current of 0A).

4. Grounds 4-5 disclose pre-regulated input voltage (POR 69-71)

The Petition correctly identifies a “*pre-regulated input voltage*”⁵ to each converter. Pet. 126-27. Netlist argues that “the 5V system voltage is not directly received by the 5V-to-3.3V regulator 184,” POR 69, but that ignores the 918 Patent’s implementation of indirect connection to the input voltage shown below (pp.34-35), and is incorrect as discussed above (p.31, note 4). Furthermore, as Dr. Wolfe explained, the on-board 3.3V can be generated by “another, similar voltage converter” during normal operation. EX1003, ¶¶691, 695.

5. Claim 23 (POR 71-72)

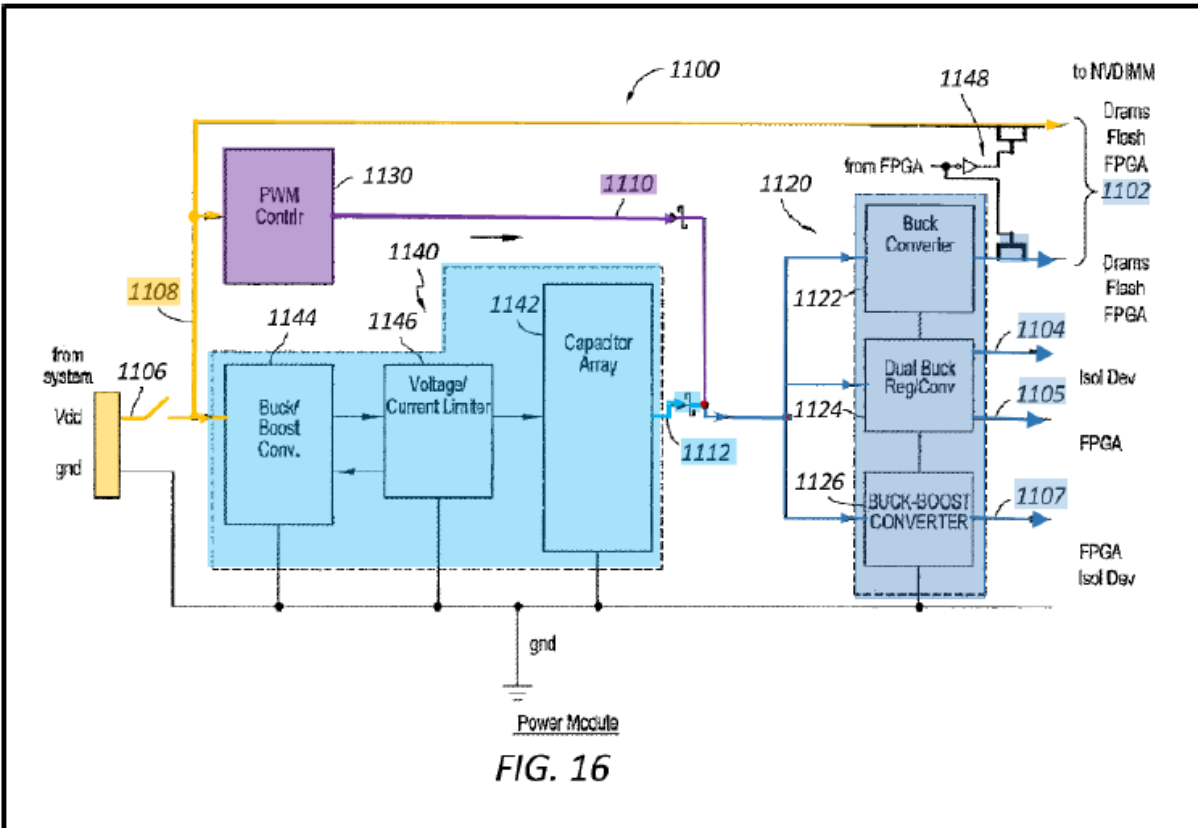
Netlist argues that Grounds 4-5 fail to satisfy “a ‘second’ voltage...selectively switched on or off” as required by claim 23. POR 71. But as correctly found by the Board, the related discussion for claim 8.b.3 shows this limitation would be obvious for at least two reasons. ID 53; Pet. 112-15. Netlist argues “Petitioner has not presented any situation in Spiers where the processor core would be off but the SDRAM remains on,” POR 72, but that ignores the situation where “to conserve power during S3 sleep mode...the SDRAMs are in self-refresh mode and power to the processor is turned off,” Pet. 112; EX1003,

⁵ See p.20, note 3.

¶¶820-22.

6. Claim 13 (POR 72-73)

For claim 13, the Petition’s voltage mappings are not limited to a “power failure,” as suggested by Netlist. POR 72 (citing Pet. 86). Spiers’s power supply components (including regulator 184) connect to the 5V supply voltage even during normal operation, as explained above (p.31, note 4). Netlist ignores that Spiers’s card “uses the ‘+5 volt’ power supply of the PCI bus to power components of the card.” EX1003, ¶¶657-99. Furthermore, Netlist’s argument appears to rest on an overly narrow view of what “coupled to” requires in claim 13, *see* EX2030, 278:17-279:24, which would exclude the preferred embodiment (where the “input voltage” 1106, below left, is *indirectly* connected through 1130/1140 (purple/blue) to the buck converters 1122, 1124, 1126 on the right):

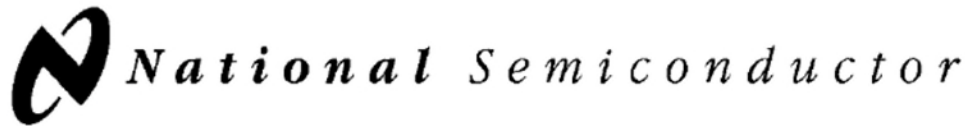


EX1001, Fig.16; EX1075, 120:10-121:22.

7. Claims 5-7, 9-13, 16-22, 24-27 (POR 73-75)

Grounds 4-5, like Grounds 2-3, show that *over*voltage protection was obvious in light of Amidi and Hajeck. Pet. 102-08, 128-30. Netlist repeats for Grounds 4-5 the same arguments discussed above (pp.20-22). POR 73-75. Contrary to Netlist's arguments, POR 74, Spiers is not limited to switching to backup power in case of *under*voltage, but concerns "power failure, or other failure" in general, *see* EX1025, Fig.14 (step 720, "Power Fail Detect"), [0030] ("store the data in a non-volatile memory, such that if a power failure, *or other failure*, occurs"). In fact, Spiers discloses a PCI 5V voltage detector 202, *see id.*

Figs.5, 14, [0037], and such commercially available detectors included **both** under and overvoltage detection, *see* Pet. 104-05; EX1063, pp.1-2 (below); EX1003, ¶¶767-78.



LMC6953

PCI Local Bus Power Supervisor

DC Electrical Characteristics

Unless otherwise specified, all **boldface** limits guaranteed for $T_J = 0^{\circ}\text{C}$ to 70°C , $V_{DD} = 5\text{V}$, $R_{PULL-UP} = 4.7\text{ k}\Omega$ and $C_{EXT} = 0.01\text{ }\mu\text{F}$. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	(Note 4)	5.45	5.6	5.75	V
V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	4.25	4.4	4.55	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	3.8	3.95	4.1	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	2.5	2.65	2.8	V

Netlist argues that detecting overvoltage does not render obvious switching to backup power, POR 74, but that ignores the dangers of losing data (or damaging the circuit) due to the overvoltage, as discussed above (pp.20-22). Netlist also argues that, instead of Spiers's power circuit, Hajeck's **charge pump** could be used, POR 75, but that charge pump could handle only "a **brief** interruption, drop, increase, or spike in the voltage V_{IN} ," EX1038, 3:2-:6; EX2030, 226:16-:22, 230:17-232:6, 251:10-254:2. In any event, the existence of an alternative does not make switching to backup power non-obvious, certainly not in "mission critical" systems relying on "irreplaceable data" as taught by Amidi. EX1024, 1:19-:20.

And, of course, Hajeck's charge pump cannot operate "indefinitely" for all possible power anomalies. EX1075, 197:14-198:5.

Netlist also repeats its argument that the prior art does not teach a write operation in response to a trigger signal for an over-voltage event. POR 75. This argument is incorrect for the reasons stated above (p.23).

8. Registered plurality of C/A signals for claims 8, 14 (POR 75-76)

Netlist argues that Spiers's processor "translat[es]" the signals from the host to the SDRAMs, and thus supposedly does not "register[]" them. POR 75-76. But in order to "translate" those signals, Spiers's processor would first need to "capture" and thus "register" those signals, Pet. 108-12; EX1003, ¶807, as was standard, EX1075, 91:1-93:16; EX1077, 8. Nothing in the claims requires a direct pass-through of "registered" signals without translation, which would exclude preferred embodiments like FBDIMM (pp.8-9).

III. CONCLUSION

For the reasons set forth above and in the Petition, Samsung respectfully requests that claims 1-30 be canceled as unpatentable.

Dated: June 20, 2023

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CERTIFICATE OF COMPLIANCE

I hereby certify that this **Petitioner's Reply to Patent Owner's Response** complies with the type-volume limitations of 37 C.F.R. § 42.24(c)(1) because it contains 5,596 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the reply exempted by 37 C.F.R. § 42.24(c).

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 20th day of June, 2023, **Petitioner's Reply to Patent Owner's Response and Exhibits 1075 to 1078** were served by email on the following counsel for Patent Owner:

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